REMARKS

In an Office Action mailed September 11, 2007, pending claims 1-27 were examined and rejected after having been previously allowed. The rejection was non-final. Rather than regretting any delay in citing new references, Applicant thanks the Examiner for finding previously uncited prior art which has provided the opportunity to issue claims of the correct scope. In response to the rejection, Applicant has amended claims 1-6, 8-10, 12-16, 18 and 24. Applicant respectfully requests the allowance of claims 1-27 thereby placing the application in condition for allowance.

Claims 1-27 were rejected under 35 U.S.C. 102(e) as being anticipated by DeBrosse et al. (U.S. Patent 6,704,230). DeBrosse et al. in FIG. 2 disclose an MRAM that selectively refreshes the storage area in response to a count value of a counter of a refresh mechanism external to the storage area. It should be noted that the MRAM taught by DeBrosse et al. is not a toggle MRAM. To write a memory bit of a toggle MRAM the present state of the addressed memory bit is compared with a new bit value to be written. Depending upon the comparison result, the bit may not be magnetically reversed if no change is needed.

Independent claims 1, 8 and 18 are herein amended to more particularly distinguish the claimed subject matter. For example, DeBrosse et al. do not teach or suggest "providing a count of occurrences of the error signal for storage in the reserved portion of the magnetoresistive random access memory (MRAM) core by using an unused portion of a write memory cycle during a read operation to implement said storage" as recited in claim 1. In the recited

memory a count of how many errors associated with the memory operation may be readily known by reading the MRAM core which is nonvolatile. This functionality is not present in the DeBrosse et al. circuit and the count value is lost if power to the DeBrosse et al. circuit is removed. Additionally, there is no teaching or suggestion by Debrosse et al. of the efficient storage of an error count in an MRAM by "using an unused portion of a write memory cycle during a read operation to implement said storage". The recited memory of claim 1 is efficient in storing the count value in the recited MRAM core and not requiring a dedicated memory cycle solely to store an error count value. Thus the recited memory provides a user with an efficient way to read an error count when the memory is in any operating mode. Further, DeBrosse et al. do not teach or suggest the recited "write cycle counter" and "read cycle counter" in apparatus claims 1-17 and do not teach the recited storage of write and read cycles in the MRAM core recited in method claims 18-24. DeBrosse et al. do not teach or suggest "using an unused portion of a write memory cycle during a read operation" as recited in method claims 18-24 in connection with storing counts of detected errors, write cycles and read cycles.

The block 265 of the DeBrosse et al. was stated to be a "write cycle counter", a "read cycle counter" and an "error counter" on page 3 of 10 of the Office Communication. The citation of DeBrosse et al. at Col. 6, lines 60-63 was provided in support of this position. However, counting a number of read cycles and a number of write cycles is not taught by DeBrosse et al. The claim 1 recitation enables errors occurring during a known number of write and/or read cycles to be monitored and this is not taught or suggested by DeBrosse et al. At Col. 6, lines 50-63 of DeBrosse et al. that was cited in the Office Action, DeBrosse et al. teach the use of multiple error counters for

refresh monitoring purposes. In this section DeBrosse et al. also teach not refreshing the memory when no errors are counted in a specific time period. There is however no teaching or suggestion of counting write cycles and counting read cycles, no teaching or suggestion of storing that information in an MRAM core or how to do so in an efficient manner.

The other independent claims 8 and 18 are herein amended to recite many of these distinguishing features. The dependent claims are distinguishable from the DeBrosse et al. patent at least for these reasons. In addition it should be noted that many of the additional features in the dependent claims are not taught or suggested by DeBrosse et al. As mentioned above, the DeBrosse et al. memory is not a toggle memory as recited in claims 2 and 9 and DeBrosse et al. do not teach or suggest a toggle operation as recited in claim 22. The length of write and read cycles is not taught by DeBrosse et al. as recited, for example, in claims 4 and 5. Therefore, Applicant respectfully requests the reconsideration and withdrawal of the rejection of claims 1-27 on the basis of DeBrosse et al.

Claims 1-2, 8-9 and 18-19 were rejected under 35 U.S.C. 102(e) as being anticipated by Perner et al. (U.S. Patent 6,584,589). In response Applicant has amended each of independent claims 1, 8 and 18. Perner et al. discloses an MRAM array that is not a toggle array. At Col. 14, lines 51-53 Perner et al. clearly discuss a write operation regarding how a data bit is programmed by asserting pull-up and pull-down transistors to assert a selected binary state. No toggle operation is taught by Perner et al. Additionally, no error count data, write cycle count or read cycle count is stored in the memory array. Thus Perner et al. do not disclose the recited "write cycle counter" and

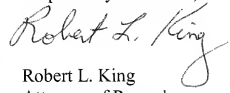
"read cycle counter" of claim 1 or the recited "providing a count of occurrences of the error signal for storage in the reserved portion of the magnetoresistive random access memory (MRAM) core by using an unused portion of a write memory cycle during a read operation to implement said storage" of claim 1. Perner et al. does not disclose the recited "read cycle counter" and the "write cycle counter" nor the "storage in the non-volatile random access memory (NVRAM) core by using an unused portion of a write memory cycle during a read operation to implement said storage" as recited in claim 8. Perner et al. do not disclose "obtaining a count of detected errors, a count of write cycles and a count of read cycles" as recited in claim 18. Dependent claims 2, 9 and 19 are allowable over the Perner et al. patent for at least these reasons.

The rejection basis on page 7 of 10 of the Office Action stated that Perner et al. taught block 101 as an error counter. Applicant assumes that the Examiner meant block 110 of the Perner et al. patent drawings. At Col. 4, line 7-9 the Perner et al. patent states that counter 110 is a column error counter which is coupled to a separate test circuit 108 and not the MRAM memory array. Therefore, the counter is not counting errors associated directly in the MRAM array but rather errors found in a separate test circuit 108. From the citation at Col. 15, lines 30-45 that was provided in the Office Communication, it is evident that the error count is provided to external circuits (Col. 15, line 42) in the context of a BIST which requires a special test mode for the circuitry to be in. The limitations discussed above in connection with amended independent claims 1, 8 and 18 readily distinguish the pending claims from the teachings of Perner et al. Therefore, Applicant requests the

reconsideration and withdrawal of the rejection of claims 1, 2, 8, 9, 18 and 19 and the allowance thereof.

Applicant requests the allowance of the pending application. Should issues remain that might be subject to resolution through a telephonic interview, the Examiner is requested to telephone the undersigned at (512) 996-6839.

Respectfully submitted,



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